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(71) Applicant *(for all designated States except US)*: **TOKYO ELECTRON DEVICE LIMITED** [JP/JP]; 1, Higashikata-cho, Tsuzuki-ku, Yokohama-shi, Kanagawa 224-0045 (JP).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **MURAKAMI, Kazuaki** [JP/JP]; 1-2-307, Kasugakoen 4-chome,, Kasuga-shi, Fukuoka 816-0811 (JP). **KIKUCHI, Syuichi** [JP/JP]; c/o Tokyo Electron Device Limited,, Basyonotsuji Building, 3-16, Ichiban-cho 3-chome, Aoba-Ku, Sendai-Shi, Miyagi 980-0811, (JP).

(74) Agent: **KIMURA, Mitsuru**; 2nd Floor, Kyohan Building, 7, Kandanishiki-cho 2-chome, Chiyoda-ku, Tokyo 101-0054 (JP).

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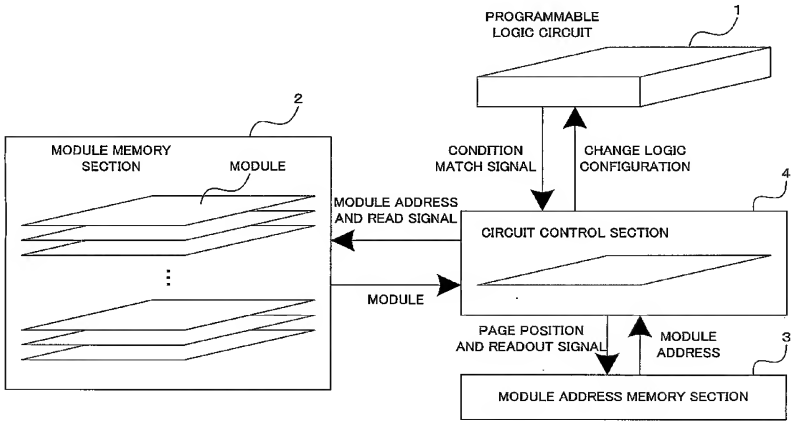

(57) Abstract: Disclosed is a programmable logic circuit control apparatus and method, and a program, which facilitate smooth execution of multiple processes in complicated procedures. A module address memory section (3) stores data indicating the address of a module to be read by a circuit control section (4) or a condition for a branch process and a jump distance for each page. The circuit control section (4) reads data stored on the topmost page in the module address memory section (3). According to the data, the circuit control section (4) performs reading of a module, reconfiguration of a programmable logic circuit (1) and reading of data of the next page, or jumps. Every time a new page is read, the circuit control section (4) performs processes according to data stored on that page, thereby sequentially reconfiguring the programmable logic circuit (1).

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DESCRIPTION

PROGRAMMABLE LOGIC CIRCUIT CONTROL APPARATUS, PROGRAMMABLE LOGIC CIRCUIT CONTROL METHOD AND PROGRAM

Technical Field

The present invention relates to a programmable logic circuit control apparatus, a programmable logic circuit control method and a program.

Background Art

In fields where ASICs (Application Specific Integrated Circuits) are used, there is a demand of flexible adaptation to changes in specifications during development of an ASIC, and shortening the development stage of a product. To meet the demand, programmable logic circuits, such as a field programmable gate array (FPGA) (e.g., XC series by XILINX in U.S.A.) and a programmable logic device (PLD), are widely used. A programmable logic circuit can freely change the logic configuration of an internal logic circuit according to circuit information loaded.

Recently, logic configurations demanded of ASICs are becoming complex, and the scales of ASICs are becoming larger. Accordingly, there is a case where construction of an ASIC is constructed by using programmable logic circuits, therefore, several programmable logic circuits to several scores of programmable logic circuits are used in some case.

Paying attention to the fact that not all the parts of a large-scale logic circuit are always operating, several schemes of designing an ASIC smaller are proposed. The schemes reconfigure a programmable logic circuit in such a way that the same programmable logic circuit achieves different functions at different times (see Unexamined Japanese Patent Application KOKAI Publications Nos. 2001-202236, 2003-198362 and 2003-029969, for example). The schemes can make the scale of an ASIC smaller by

reconfiguring a programmable logic circuit.

However, complex ASICs do not just execute processes one after another. ASICs are generally expected to execute a process in complicated procedures including conditional branching, returning from a branched step and loops. The aforementioned schemes of reconfiguring a programmable logic circuit face a difficulty in smoothly executing multiple processes in such complicated procedures and suffer a long overhead.

Disclosure of Invention

Accordingly, it is an object of the present invention to provide a programmable logic circuit control apparatus, a programmable logic circuit control method and a program, which facilitate smooth execution of multiple processes in complicated procedures.

To achieve the object, a programmable logic circuit control apparatus according to the first aspect of the invention comprises:

a controller (4) which supplies a control signal to an external programmable logic circuit (1) having a function of changing a logic configuration in accordance with a supplied control signal;

a module storage memory (2) which stores a plurality of modules each comprised of data defining a logic configuration of the programmable logic circuit (1); and

a module usage order designation memory (3) which has a plurality of ordered memory positions, each of the memory positions storing data for designating an address of a memory position of the module storage memory (2) in which a module to be executed is stored or storing data for designating an address of another memory position of this module usage order designation memory (3),

wherein the controller (4) acquires data stored at a memory position in the module usage order designation memory (3),

determines which of an address of the memory position storing the module and an address of the another memory position is designated by the acquired data,

when having determined that the acquired data designates an address of the module, acquires the module stored in a memory position indicated by the address from the module storage memory (2), generates a control signal which controls the programmable logic circuit (1) to take a logic configuration defined by the module and supplies the generated control signal to the programmable logic circuit (1), and

when having determined that the acquired data designates another memory position, acquires data stored at the another memory position from the module usage order designation memory (3).

The programmable logic circuit control apparatus easily and smoothly executes a process of changing the logic configuration of a programmable logic circuit even when the process involves complicated procedures including branch processes.

When data stored at a memory position in the module usage order designation memory (3) designates another memory position in the module usage order designation memory (3), the data may include condition definition data designating a condition to start a process of acquiring data stored at the another memory position.

The controller (4) may determine whether a condition designated by the condition definition data included in the acquired data is fulfilled or not when having determined that the acquired data designates another memory position,

may acquire data stored at the another memory position of the module usage order designation memory (3) when having determined that the condition is fulfilled, and

may abort acquisition of data at the another memory position when having determined that the condition is not fulfilled.

The logic circuit control apparatus with the structure easily and smoothly executes a process of changing the logic configuration of a programmable logic circuit even when the process involves complicated procedures including conditional branching.

The condition designated by the condition definition data may relate to a value

given by a signal which is generated at a predetermined node of the programmable logic circuit (1).

In this case, when having determined that data stored at a memory position in the module usage order designation memory (3) designates another memory position, the controller (4) may acquire the signal from the node of the programmable logic circuit (1). Based on the value given by the acquired signal, the controller (4) may determine whether that condition which is designated by the condition definition data included in the data acquired from the module usage order designation memory (3) is fulfilled or not.

Data stored at a memory position in the module usage order designation memory (3) may include identification data for identifying which one of an address of the memory position storing a module and an address of another memory position is designated by the stored data.

In this case, based on the identification data included in the data acquired from the module usage order designation memory (3), the controller (4) may determine which of an address of the memory position storing the module and an address of the another memory position is designated.

A programmable logic circuit control apparatus according to the second aspect of the invention acquires a module comprised of data defining a logic configuration of an external programmable logic circuit (1) having a function of changing a logic configuration in accordance with a supplied control signal from a module storage memory (2) which stores a plurality of modules, generates a control signal which controls the programmable logic circuit (1) to take a logic configuration defined by the acquired module and supplies generated control signal to the programmable logic circuit (1), and comprises:

means which acquires data stored at a memory position in an external module usage order designation memory (3) which has a plurality of ordered memory positions, each of the memory position storing data for designating an address of a memory position of the

module storage memory (2) in which a module to be executed is stored or storing data for designating an address of another memory position of this module usage order designation memory (3), from the module usage order designation memory (3);

means which determines which of an address of the memory position storing the module and an address of the another memory position is designated by acquired data;

means which, when it is determined that the acquired data designates an address of the module, acquires the module stored in a memory position indicated by the address from the module storage memory (2), and changes the logic configuration of the programmable logic circuit (1) so that the programmable logic circuit (1) takes a logic configuration defined by the module; and

means which, when it is determined that the acquired data designates another memory position, acquires data stored at the another memory position from the module usage order designation memory (3).

This programmable logic circuit control apparatus also easily and smoothly executes a process of changing the logic configuration of a programmable logic circuit even when the process involves complicated procedures including branch processes.

A programmable logic circuit control method according to the third aspect of the invention supplies a control signal to an external programmable logic circuit (1) having a function of changing a logic configuration in accordance with the supplied control signal, and comprises the steps of:

storing a plurality of modules each comprised of data defining a logic configuration of the programmable logic circuit (1);

storing data for designating an address of a memory position storing a module or an address of another memory position at each of a plurality of ordered memory positions;

acquiring data stored at each of the memory positions;

determining which of an address of the memory position storing the module and an

address of the another memory position is designated by the acquired data;

when it is determined that the acquired data designates an address of a memory position storing a module, acquiring the module stored in the memory position indicated by the address, generating a control signal which controls the programmable logic circuit (1) to take a logic configuration defined by the module and supplying the control signal to the programmable logic circuit (1); and

when it is determined that the acquired data designates an address of another memory position, acquiring data stored at the another memory position.

The programmable logic circuit control method easily and smoothly executes a process of changing the logic configuration of a programmable logic circuit even when the process involves complicated procedures including branch processes.

A programmable logic circuit control method according to the fourth aspect of the invention acquires a module comprised of data defining a logic configuration of an external programmable logic circuit (1) having a function of changing a logic configuration in accordance with a supplied control signal from a module storage memory (2) which stores a plurality of modules, generates a control signal which controls the programmable logic circuit (1) to take a logic configuration defined by the acquired module and supplies the control signal to the programmable logic circuit (1), and comprises the steps of:

acquiring data stored at a memory position in an external module usage order designation memory (3) which has a plurality of ordered memory positions, each of the memory positions storing data for designating an address of a memory position of the module storage memory (2) in which a module to be executed is stored or storing data for designating an address of another memory position of this module usage order designation memory (3);

determining which of an address of the memory position storing the module and an address of the another memory position is designated by the acquired data;

when it is determined that the acquired data designates an address of a memory position storing a module, acquiring the module stored in the memory position indicated by the address from the module storage memory (2), and changing the logic configuration of the programmable logic circuit (1) so that the programmable logic circuit (1) takes a logic configuration defined by the module; and

when it is determined that the acquired data designates another memory position, acquiring data stored at the another memory position from the module usage order designation memory (3).

This programmable logic circuit control method also easily and smoothly executes a process of changing the logic configuration of a programmable logic circuit even when the process involves complicated procedures including branch processes.

A program according to the fifth aspect of the invention allows a computer to function as:

a controller (4) which supplies a control signal to an external programmable logic circuit (1) having a function of changing a logic configuration in accordance with the supplied control signal;

a module storage memory (2) which stores a plurality of modules each comprised of data defining a logic configuration of the programmable logic circuit (1); and

a module usage order designation memory (3) which has a plurality of ordered memory positions, each of the memory positions storing data for designating an address of a memory position of the module storage memory (2) in which a module to be executed is stored or storing data for designating an address of another memory position of the module usage order designation memory (3),

wherein the controller (4) acquires data stored at a memory position in the module usage order designation memory (3),

determines which of an address of the memory position storing the module and an

address of the another memory position is designated by the acquired data,

when having determined that the acquired data designates an address of a module, acquires the module stored in a memory position indicated by the address from the module storage memory (2), generates a control signal which controls the programmable logic circuit (1) to take a logic configuration defined by the module and supplies the generated control signal to the programmable logic circuit (1), and

when having determined that the acquired data designates another memory position, acquires data stored at the another memory position from the module usage order designation memory (3).

A computer which executes the program easily and smoothly executes a process of changing the logic configuration of a programmable logic circuit even when the process involves complicated procedures including branch processes.

A program according to the sixth aspect of the invention allows a computer to function as a programmable logic circuit control apparatus that acquires a module comprised of data defining a logic configuration of an external programmable logic circuit (1) having a function of changing a logic configuration in accordance with a supplied control signal from a module storage memory (2) which stores a plurality of modules, generates a control signal which controls the programmable logic circuit (1) to take a logic configuration defined by the acquired module and supplies generated control signal to the programmable logic circuit (1), and further allows the computer to perform the functions of:

acquiring data stored at a memory position in an external module usage order designation memory (3) which has a plurality of ordered memory positions, each of the memory positions storing data for designating an address of a memory position of the module storage memory (2) in which a module to be executed is stored or storing data for another memory position of this module usage order designation memory (3);

determining which of an address of the memory position storing the module and an

address of the another memory position is designated by acquired data;

when it is determined that the acquired data designates an address of a module, acquiring the module stored in a memory position indicated by the address from the module storage memory (2), and changing the logic configuration of the programmable logic circuit (1) so that the programmable logic circuit (1) takes a logic configuration defined by the module; and

when it is determined that the acquired data designates another memory position, acquiring data stored at the another memory position from the module usage order designation memory (3).

A computer which executes the program also easily and smoothly executes a process of changing the logic configuration of a programmable logic circuit even when the process involves complicated procedures including branch processes.

As apparent from the above, the present invention realizes a programmable logic circuit control apparatus and method, and a program, which facilitate smooth execution of multiple processes in complicated procedures.

Brief Description of Drawings

These objects and other objects and advantages of the present invention will become more apparent upon reading of the following detailed description and the accompanying drawings in which:

FIG. 1 is a diagram illustrating the structure of a programmable logic circuit control apparatus according to one embodiment of the present invention;

FIG. 2 is an exemplary diagram showing the configuration of a programmable logic circuit;

FIG. 3 is a diagram showing the configuration of an input logic circuit BIBC;

FIG. 4 is a diagram showing the configuration of a logic circuit BFBC;

FIG. 5 is a diagram showing the configuration of a logic circuit BQBC;

FIG. 6 is a diagram showing the configuration of an output logic circuit BOBC;

FIG. 7A is a diagram showing the structure of a matrix switch, and FIG. 7B is a diagram showing the structure of switches which constitutes the matrix switch;

FIG. 8 is an exemplary diagram showing the data structure of data stored in a module address memory section; and

FIG. 9 is a flowchart illustrating the flow of a process which is executed by a circuit control section.

Best Mode for Carrying Out the Invention

A preferred embodiment of the present invention, as adapted to a programmable logic circuit control apparatus, will be described below with reference to the accompanying drawings.

FIG. 1 illustrates the structure of the programmable logic circuit control apparatus. The programmable logic circuit control apparatus includes a programmable logic circuit 1, a module memory section 2, a module address memory section 3, and a circuit control section 4. The programmable logic circuit 1, the module memory section 2 and the module address memory section 3 are connected to the circuit control section 4.

The programmable logic circuit 1 is comprised of a configurable logic block (CLB), which is used to construct, for example, a field programmable gate array (FPGA) produced by XILINX in U.S.A., a matrix switch, a wiring material and so forth. The programmable logic circuit 1 changes (reconfigures) its logic configuration (i.e., the correlation between signals to be input to the programmable logic circuit 1 and signals to be output therefrom) under the control of the circuit control section 4. As exemplified in FIG. 2, for example, the programmable logic circuit 1 includes input logic circuits BIBC, logic circuits BFBC, logic circuits BQBC, output logic circuits BOBC, a matrix switche BLSW, wires LVL0 to LVL4 and wires LHL0 to LHL2.

Each of the wires LVL0 to LVL4 and the wires LHL0 to LHL2 consists of 63 signal

lines. The input logic circuits BIBC, the logic circuits BFBC, the logic circuits BQBC and the output logic circuits BOBC are connected to the wires LVL0 to LVL4 via buses. The wires LVL0 to LVL4 and the wires LHL0 to LHL2 are connected to one another or disconnected from one another by the matrix switch BLSW. The matrix switch BLSW realizes variable interconnection.

Each of the input logic circuit BIBC, the logic circuit BFBC, the logic circuit BQBC and the output logic circuit BOBC is constituted by, for example, a TTL (Transistor-Transistor Logic) circuit or a CMOS (Complementary Metal-Oxide Semiconductor) logic circuit or so.

Each input logic circuit BIBC supplies a signal input to the programmable logic circuit 1 to the wire LVL0 in a mode according to the control of the circuit control section 4. Each input logic circuit BIBC is comprised of, for example, an output select circuit OSEL1 as shown in FIG. 3.

The output select circuit OSEL1 is connected to the wire LVL0 via buses IoA(1) to IoA(63) of 63 bits. The output select circuit OSEL1 supplies a 4-bit signal input to the programmable logic circuit 1 to the signal lines constituting the wire LVL0. Based on the value of a 24-bit control signal ConfigI supplied from the circuit control section 4 or so, the output select circuit OSEL1 decides to which signal line in the wire LVL0 the signal is to be supplied. The output select circuit OSEL1 then sends the signal to the decided signal line. The output select circuit OSEL1 can decide not to send the signal to any of the signal lines of the wire LVL0.

Each logic circuit BFBC performs a logical operation on a signal supplied from the wire LVL0 or LVL1 under the control of the circuit control section 4. The logic circuit BFBC sends the acquired signal to the wire LVL1 or LVL2. Each logic circuit BFBC includes, for example, an input select circuit ISEL1, a basic function cell FBC and an output select circuit OSEL2 as shown in FIG. 4.

The input select circuit ISEL1 is connected to the wire LVL0 or LVL1 via buses IiA(1) to IiA(63) of 63 bits. The input select circuit ISEL1 acquires a 6-bit signal among signals supplied from the wire LVL0 or LVL1 to which the input select circuit ISEL1 is connected. The input select circuit ISEL1 sends the acquired signal to the basic function cell FBC. Based on the value of a 36-bit control signal ConfigFi supplied from the circuit control section 4 or so, the input select circuit ISEL1 decides from which six signal lines in the 63 signal lines of the wire LVL0 or LVL1 the signal is to be acquired. The input select circuit ISEL1 acquires the signal from the decided signal lines. The input select circuit ISEL1 then sends the acquired signal to the basic function cell FBC. The input select circuit ISEL1 can decide not to acquire a signal from any of the signal lines of the wire LVL0 or LVL1. In this case, the input select circuit ISEL1 sends a signal representing a logic value "0" to the basic function cell FBC.

The basic function cell FBC includes, for example, a select circuit SEL and a latch circuit L as shown in FIG. 4.

Based on the value of the 6-bit signal supplied from the input select circuit ISEL1, the basic function cell FBC selects a total of two bits, one bit from the first to 64-th bits of a 130-bit control signal ConfigFf supplied from the circuit control section 4 or so, and one bit from the 65-th to 128-th bits of the control signal ConfigFf. The basic function cell FBC sends the 2-bit signal (signal XY) to the output select circuit OSEL2. Based on the values of the 129-th and 130-th bits of the control signal ConfigFf, the basic function cell FBC decides whether or not to latch the signal XY. The basic function cell FBC then sends a signal EN indicating the result of the decision to the latch circuit L.

Based on the signal EN, the latch circuit discriminates whether or not it is decided to latch the signal XY. When it is decided to latch the signal XY, the latch circuit L holds the value of the signal XY. Then, the latch circuit L sends a 2-bit signal having the held value to the output select circuit OSEL2 as a signal QY. When it is not decided to latch the

signal XY, on the other hand, the latch circuit L sends a 2-bit signal having a value currently held (i.e., the old value of the signal XY) to the output select circuit OSEL2 as the signal QY. At the time of latching the signal XY, the individual sections of the programmable logic circuit 1 perform latching in synchronism with a clock signal. The programmable logic circuit 1 may acquire the clock signal externally. Alternatively, the programmable logic circuit 1 may have a circuit to generate the clock signal.

The output select circuit OSEL2 is connected to the wire LVL1 or LVL2 via buses IoB(1) to IoB(63) of 63 bits. The output select circuit OSEL2 supplies the signal XY and the signal QY, a total of four bits, supplied from the basic function cell FBC to the signal lines constituting the wire LVL1 or LVL2. The output select circuit OSEL2 decides to which signal line in the wire LVL1 or LVL2 the 4-bit signal is to be supplied, based on the value of a 24-bit control signal ConfigFo supplied from the circuit control section 4 or so. The output select circuit OSEL2 then sends the 4-bit signal to the decided signal line. The output select circuit OSEL2 can decide not to send the signal to any of the signal lines of the wire LVL1 or LVL2.

Each logic circuit BQBC holds a signal supplied from the wire LVL2 or LVL3 in a mode according to the control of the circuit control section 4. The logic circuit BQBC gives the signal to the logic circuit BFBC in the programmable logic circuit 1 after reconfigure to a next logic configuration via the wire LVL0 or LVL1. Each logic circuit BQBC includes, for example, an input select circuit ISEL2, a function cell QBC and an output select circuit OSEL3 as shown in FIG. 5.

The input select circuit ISEL2 is connected to the wire LVL2 or LVL3 via buses IiB(1) to IiB(63) of 63 bits. The input select circuit ISEL2 acquires a 4-bit signal among signals supplied from the wire LVL2 or LVL3 to which the input select circuit ISEL2 is connected. The input select circuit ISEL2 sends the acquired signal to the function cell QBC. Based on the value of a 24-bit control signal ConfigQi supplied from the circuit

control section 4 or so, the input select circuit ISEL2 decides from which four signal lines in the 63 signal lines of the wire LVL2 or LVL3 the signal is to be acquired. The input select circuit ISEL2 acquires signals of a total of four bits from the decided signal lines, and sends the acquired signal to the function cell QBC. The input select circuit ISEL2 can decide not to acquire a signal from any of the signal lines of the wire LVL2 or LVL3. In this case, the input select circuit ISEL2 sends a signal representing a logic value "0" to the function cell QBC.

The function cell QBC is comprised of a latch circuit or so. The function cell QBC holds the value of a 4-bit signal supplied from the input select circuit ISEL2. The function cell QBC sends a signal having the held value to the output select circuit OSEL3 as a signal QY2.

The output select circuit OSEL3 is connected to the wire LVL3 or LVL4 via buses IoC(1) to IoC(63) of 63 bits. The output select circuit OSEL3 supplies the 4-bit signal QY2 supplied from the function cell QBC to the signal lines constituting the wire LVL3 or LVL4. The output select circuit OSEL3 decides to which signal line in the wire LVL3 or LVL4 the signal QY2 is to be supplied, based on the value of a 24-bit control signal ConfigQo supplied from the circuit control section 4 or so. The output select circuit OSEL3 then sends the signal to the decided signal line. The output select circuit OSEL3 can decide not to send the signal to any of the signal lines of the wire LVL3 or LVL4.

Each output logic circuit BOBC outputs a signal supplied from the wire LVL4 in a mode according to the control of the circuit control section 4. Each output logic circuit BOBC includes, for example, an input select circuit ISEL3 and a function cell OBC as shown in FIG. 6.

The input select circuit ISEL3 is connected to the wire LVL4 via buses IiC(1) to IiC(63) of 63 bits. The input select circuit ISEL3 acquires a 4-bit signal among signals supplied from the wire LVL4 to which the input select circuit ISEL3 is connected. The

input select circuit ISEL3 sends the acquired signal to the function cell OBC. Based on the value of a 24-bit control signal ConfigO supplied from the circuit control section 4 or so, the input select circuit ISEL3 decides from which four signal lines in the 63 signal lines of the wire LVL4 the signal is to be acquired. The input select circuit ISEL3 acquires signals of a total of four bits from the decided signal lines, and sends the acquired signal to the function cell OBC. The input select circuit ISEL3 can decide not to acquire a signal from any of the signal lines of the wire LVL4. In this case, the input select circuit ISEL3 sends a signal representing a logic value "0" to the function cell OBC.

The function cell OBC is comprised of a latch circuit or so. The function cell OBC holds the value of a 4-bit signal supplied from the input select circuit ISEL3 or passes this signal. Whether to hold or pass the signal is decided based on the 25-th to 28-th bits in the control signal ConfigO. The function cell OBC sends out a signal having the held value or the signal that has passed as an output signal (signal Y) of the programmable logic circuit 1.

The matrix switch BLSW has a capability of electrically connecting or disconnecting the wires LVL0 to LVL4 and the wires LHL0 to LHL2 to one another or from one another. The matrix switch BLSW electrically connects or disconnects the wires LVL0 to LVL4 from one another, electrically connects or disconnects the wires LHL0 to LHL2 from one another, or electrically connects or disconnects the wires LVL0 to LVL4 to or from the wires LHL0 to LHL2 in accordance with a value of a control signal (hereinafter the control signal will be referred to as control signal ConfigL) supplied from the circuit control section 4, etc.

As shown in FIG. 7A, for example, the matrix switch BLSW, which connects or disconnects wires LVLm (m being an integer from 0 to 4) to or from wires LHLn (n being an integer from 0 to 2), is comprised of 3969 switches Q which connect or disconnect wires LVLm-j (j being an integer from 1 to 63) to or from wires LHLn-k (k being an integer from 1 to 63). Each switch Q is comprised of a switching element, such as field effect transistor

(FET), for example, as shown in FIG. 7B. In the example illustrated in FIG. 7, a FET Q1 connects or disconnects two signal lines LVLm-jA and LVLm-jB constituting the wire LVLm-j to or from each other. A FET Q2 connects or disconnects two signal lines LHLn-kA and LHLn-kB constituting wires LHLn-k to or from each other. A FET Q3 connects or disconnects the signal line LVLm-jA and the signal line LHLn-kA to or from each other. A FET Q4 connects or disconnects the signal line LVLm-jA and the signal line LHLn-kB to or from each other. A FET Q5 connects or disconnects the signal line LVLm-jB and the signal line LHLn-kA to or from each other. A FET Q6 connects or disconnects the signal line LVLm-jB and the signal line LHLn-kB to or from each other. When the switches Q has the structure as shown in FIG. 7B, a control signal ConfigL should be applied to, for example, the gate of each of the FETs constituting the switches Q.

The wires LVL0 to LVL4 are connected to the input logic circuits BIBC, the logic circuits BFBC, the logic circuits BQBC and the output logic circuits BOBC. The wires LHL0 to LHL2 are connected to the matrix switch BLSW. The wires LHL0 to LHL2 are not directly connected to the input logic circuits BIBC, the logic circuits BFBC, and the logic circuits BQBC (though the wires LHL0 to LHL2 may be connected to those circuits via the matrix switch BLSW).

As the matrix switch BLSW has the above-described capability, the wiring in the programmable logic circuit 1 changes based on the control signal ConfigL supplied to the matrix switch BLSW from the circuit control section 4 or so. The input logic circuits BIBC, the logic circuits BFBC, and the logic circuits BQBC are connected to one another via the wires LVL0 to LVL4 and the wires LHL0 to LHL2 under the control of the circuit control section 4 or so. As a result, the programmable logic circuit 1 as a whole becomes a logic circuit which has a capability of executing predetermined processes that are determined by the contents of modules to be discussed later.

Each of the module memory section 2 and the module address memory section 3 is

comprised of a memory, such as a RAM (Random Access Memory). Each of the module memory section 2 and the module address memory section 3 reads out data (to be discussed) stored therein in response to an access made by the circuit control section 4. The module memory section 2 and the module address memory section 3 sends the read data to the circuit control section 4.

The module memory section 2 stores data (hereinafter called "module") which defines the logic configuration of the programmable logic circuit 1 as exemplified in FIG. 1. A single module indicates the whole of or a part of the logic configuration that one programmable logic circuit 1 can express at a time. A module may indicate all the logic configurations of the input logic circuits BIBC, the logic circuits BFBC, the logic circuits BQBC and the output logic circuits BOBC as shown in FIG. 2. Alternatively, a module may be for reconfiguration of a part of the logic circuit BFBC or a part of the logic circuit BQBC, without changing the logic configurations of the other logic circuits, as per the apparatus as disclosed in, for example, Unexamined Japanese Patent Application KOKAI Publication No. 2003-198362 or Unexamined Japanese Patent Application KOKAI Publication No. 2003-029969.

A 10-bit address is assigned to each of memory positions indicating memory areas in the module memory section 2. The module memory section 2 specifies a module by specifying the address of the module, i.e., the address of the top memory position (or a given part in the module, such as the end) at which the module is stored.

As shown in FIG. 8, every 16 bits of the memory area of the module address memory section 3 constitutes one page. A page address (page position) is assigned to that page. The individual pages of the module address memory section 3 are ordered from a higher page to a lower page. The 16 bits that constitutes each page are likewise ordered from a higher significant bit to a lower one.

Each page in the module address memory section 3 whose data structure is

exemplified in FIG. 8 stores the address of each module stored in the module memory section 2 or a value indicating a jump distance (offset value) in case of performing branching, and six bits of a control bit. In the example shown in FIG. 7, the address of a module or an offset value occupies the lower ten bits of each page. The control bit occupies the upper six bits.

The control bit consists of two bits indicating, for example, whether or not to allow the circuit control section 4 to perform a branch process (hereinafter called "branch control bit") and four bits indicating a branch condition in case of performing a branch process (hereinafter called "branch condition definition control bit").

When the branch control bit takes a predetermined value (e.g., a binary value of "10") and a condition specified by the branch condition definition control bit included in the same page as the branch control bit is fulfilled, the branch control bit instructs the circuit control section 4 to jump by the offset value stored in the page with the page address of the page as a start point. That is, in that case, the circuit control section 4 reads data stored on a page having the page address that is equivalent to the sum of the page address of the start page and the offset value stored on that page (i.e., data stored on the page to be jumped).

When the branch control bit takes a value other than the predetermined value (e.g., a binary value of "00" or "01"), on the other hand, the branch control bit instructs the circuit control section 4 to read a module specified by the address included in the same page as the branch control bit, from the module memory section 2. The branch control bit also instructs the circuit control section 4 to reconfigure the programmable logic circuit 1 as indicated by the read module. Further, the branch control bit instructs the circuit control section 4 to read data stored on a next page to that page (specifically, a page with a page address which is the page address of the page incremented by "1").

When the branch condition definition control bit takes a binary value of "0000", for example, the branch condition definition control bit indicates "signal Cond(0) having a

value of "0"" as a condition for executing a jump (conditional jump).

When the branch condition definition control bit takes a binary value of "0001", for example, the branch condition definition control bit indicates "signal Cond(1) having a value of "0"" as a condition for executing a conditional jump.

When the branch condition definition control bit takes a binary value of "0010", for example, the branch condition definition control bit indicates "signal Cond(2) having a value of "0"" as a condition for executing a conditional jump.

When the branch condition definition control bit takes a binary value of "0011", for example, the branch condition definition control bit indicates "signal Cond(3) having a value of "0"" as a condition for executing a conditional jump.

When the branch condition definition control bit takes a binary value of "0100", for example, the branch condition definition control bit indicates "signal Cond(4) having a value of "0"" as a condition for executing a conditional jump.

When the branch condition definition control bit takes a binary value of "1000", for example, the branch condition definition control bit indicates "signal Cond(0) having a value of "1"" as a condition for executing a conditional jump.

When the branch condition definition control bit takes a binary value of "1001", for example, the branch condition definition control bit indicates "signal Cond(1) having a value of "1"" as a condition for executing a conditional jump.

When the branch condition definition control bit takes a binary value of "1010", for example, the branch condition definition control bit indicates "signal Cond(2) having a value of "1"" as a condition for executing a conditional jump.

When the branch condition definition control bit takes a binary value of "1011", for example, the branch condition definition control bit indicates "signal Cond(3) having a value of "1"" as a condition for executing a conditional jump.

When the branch condition definition control bit takes a binary value of "1100", for

example, the branch condition definition control bit indicates "signal Cond(4) having a value of "1"" as a condition for executing a conditional jump.

When the branch condition definition control bit takes a binary value of "0111" or "1111", for example, the branch condition definition control bit indicates a condition such that "a jump is made (a jump is made unconditionally) as long as the branch control bit included on the same page as the branch condition definition control bit has the aforementioned predetermined value".

The signals Cond(0) to Cond(4) are signals of a total of five bits to be supplied to the circuit control section 4 from the logic circuit BFBC which is executing a process of monitoring whether or not a condition is fulfilled, the logic circuit BQBC which is executing a process of holding the result of another process, or the output logic circuit BOBC which is executing a process of outputting the monitoring result. In what case the signals Cond(0) to Cond(4) are supplied from the logic circuit BFBC, the logic circuit BQBC or the output logic circuit BOBC is described in a module beforehand. Possible targets to be monitored on fulfillment of a condition include, for example, a condition for calling another process and a condition for returning to the original process from which another process has been called, besides the condition for executing a conditional jump.

The circuit control section 4 is constituted by a controller including a processor, such as a CPU (Central Processing Unit), and a non-volatile memory, such as ROM (Read Only Memory) where a program to be executed by the processor is stored. Alternatively, the controller constituting the circuit control section 4 may be comprised of an exclusive electronic circuit.

The circuit control section 4 executes, for example, a process as illustrated in FIG. 9, When the circuit control section 4 is comprised of a processor, a non-volatile memory and so forth, the process shown in FIG. 9 is carried out as the processor loads the program stored in, for example, the non-volatile memory and runs the program.

Specifically, when the circuit control section 4 starts an operation, the circuit control section 4 reads data stored on a page having the topmost page address in the module address memory section 3 (i.e., the control bit and the address of a module or the offset value) first (step S1 in FIG. 9).

Next, the circuit control section 4 discriminates whether a page from which the latest data is read from the module address memory section 3 at step S5, step S7 or step S9 to be discussed later is the last page or not, i.e., whether or not the page is a page given the lowest page address (step S2). When deciding that the page is the last one, the circuit control section 4 terminates the process.

When deciding that the page is not the last one, the circuit control section 4 discriminates which process, (a) reading of a module or (b) branching (conditional jump or unconditional jump), the control bit included in the latest data read from the module address memory section 3 indicates (step S3).

When deciding that the control bit indicates the process (a), the circuit control section 4 reads a module, specified by an address included in the latest data read from the module address memory section 3, from the module memory section 2. Then, the circuit control section 4 reconfigures the programmable logic circuit 1 in such a way as to take the logic configuration indicated by the module (step S4). At step S4, specifically, the circuit control section 4 generates, for example, the aforementioned control signals ConfigI, ConfigFi, ConfigFf, ConfigFo, ConfigQi, ConfigQo, ConfigO and ConfigL and sends the control signals to the programmable logic circuit 1 in order to reconfigure the programmable logic circuit 1.

When the process at step S4 is finished, the circuit control section 4 reads data stored on a next page to the page from which the latest data has been read, from the module address memory section 3 (step S5). Then, the circuit control section 4 returns the process to step S2.

When deciding at step S3 that the control bit indicates the process (b), on the other hand, the circuit control section 4 discriminates which process, (c) unconditional jump or (d) conditional jump, the branch condition definition control bit included in the control bit indicates (step S6). At step S6, specifically, the circuit control section 4 discriminates whether the value of the branch condition definition control bit is "0111" or "1111". When the value of the branch condition definition control bit takes either value, the circuit control section 4 decides that an unconditional jump is instructed. When the value of the branch condition definition control bit takes a value other than the two values, the circuit control section 4 decides that a conditional jump is instructed.

When deciding at step S6 that an unconditional jump is instructed, the circuit control section 4 jumps by the offset value included in the same page as the control bit (i.e., reads data stored at the page to be jumped) (step S7). Then, the circuit control section 4 returns the process to step S2.

When deciding at step S6 that a conditional jump is instructed, on the other hand, the circuit control section 4 acquires, for example, the signals Cond(0) to Cond(4) supplied from the programmable logic circuit 1 (step S8). Then, the circuit control section 4 discriminates whether the branch condition indicated by the branch condition definition control bit is fulfilled or not, based on the values indicated by the acquired signals Cond(0) to Cond(4) (step S9). When deciding that the branch condition is not fulfilled, the circuit control section 4 reads data stored on a next page to the page from which the latest data has been read, from the module address memory section 3 (step S10). Then, the circuit control section 4 returns the process to step S2. When deciding that the branch condition is fulfilled, on the other hand, the circuit control section 4 returns the process to step S7.

The programmable logic circuit 1 performs arithmetic operations according to its own logic configuration of the time when a signal supplied to the input logic circuit BIBC from outside, by using that signal or the old operation result held in the logic circuit BQBC.

Then, the programmable logic circuit 1 holds a signal indicating the operation result in the logic circuit BQBC or outputs the signal from the output logic circuit BOBC.

Through the operation, the programmable logic circuit control apparatus can execute logic configuration of the programmable logic circuit 1 in a predetermined order one after another. In addition, the programmable logic circuit control apparatus smoothly executes logic configuration in complicated procedures involving conditional branching and unconditional branching.

The structure of the programmable logic circuit control apparatus is not limited to the one described above.

For example, a single memory device may execute the functions of the module memory section 2 and the module address memory section 3.

Data which is stored in the module address memory section 3 should not necessarily take the above-described data structure. For example, the number of bits constituting one page is arbitrary. The number of bits of the address of a module, the page address, the offset value, the branch control bit or the branch condition definition control bit, and the positions in each page in the module address memory section 3 are also arbitrary.

The conditions for the circuit control section 4 to make a jump are not limited to those discussed above. For example, the condition of executing a jump should not necessarily be associated with the values of the signals Cond(0) to Cond(4). The condition may be associated with arbitrary information that is acquirable by the circuit control section 4.

The signal Cond may represent a value obtained as a result of performing a predetermined process, such as a logic operation, on the value of a signal which is generated a single node or at each of plural nodes of the programmable logic circuit 1 when at one timing or plural timings. In this case, the programmable logic circuit 1 should have a logic circuit which executes the logic operation or so.

The circuit control section 4 may execute not only a jump in the aforementioned mode (i.e., a relative jump), but also an absolute jump. In this case, for example, the branch control bit stored in the module address memory section 3 should express three kinds of instructions, for example, a relative jump, an absolute jump and no jump. When the branch control bit instructs the absolute jump, the circuit control section 4 should interpret that the address of a page to be jumped is stored on the page that includes the branch control bit, instead of an offset value. In this case, the page address of the page to be jumped is stored on the page that includes the branch control bit, instead of an offset value.

The programmable logic circuit control apparatus may further have a memory having a memory area which serves as last-in-first-out (LIFO) stack. Then, the programmable logic circuit control apparatus may use the stack to manage page addresses of pages in the module address memory section 3 in the stack, and achieve call and return functions. The call and return functions can be accomplished by, for example, the following scheme.

The control bit is so designed as to be able to include data instructing a calling process or data instructing a return process. A page to be jumped in a branch process stores the address of a module which is repeatedly used. The control bit of a page to be jumped includes data which instructs returning. At the time of calling a page to be jumped, the circuit control section 4 stores the page address of a next page to the page which is currently executed. Then, the circuit control section 4 loads data stored at a page to be jumped and reconfigures the programmable logic circuit 1. Next, the circuit control section 4 reads out a page address stored in the stack (the address of a next page to the page which has been executed before jumping), and jumps to a page indicated by the page address.

This scheme can achieve the call and return functions.

To cope with a case where a process to be executed by the programmable logic circuit 1 is processed not in synchronism with other devices or so or where the time needed

for the process is not constant, a module may define the logic configuration of the programmable logic circuit 1 in such a way as to cause the logic circuit BFBC to monitor the end of the processing by the programmable logic circuit 1, the logic circuit BQBC to hold the monitoring result, and the output logic circuit BOBC to supply data indicating the end of the process to the circuit control section 4.

When a module defines a logic configuration in such a way as to cause the programmable logic circuit 1 to execute a process which is known beforehand to terminate by a predetermined number of clocks, the module may define the logic configuration in such a way as to allow the programmable logic circuit 1 to further function as a counter to count the number of clocks of the clock signal and a logic circuit which discriminates whether the number of clocks counted by the counter has reached a predetermined number or not and supplies data indicating the end of the process to the circuit control section 4 when deciding that the number of clocks has reached the predetermined number.

The circuit control section 4, the module address memory section 3 and/or the module memory section 2 may be constructed by the programmable logic circuit 1. In this case, the programmable logic circuit control apparatus further includes a non-volatile memory device (e.g., ROM or so) which stores a module defining the logic configuration for allowing the programmable logic circuit 1 to function as, for example, the circuit control section 4, the module address memory section 3 and/or the module memory section 2. The programmable logic circuit 1 should have a control circuit or so which reads a module stored in the non-volatile memory device at a timing immediately after activation of the programmable logic circuit control apparatus and changes the logic configuration of the programmable logic circuit 1 as defined by the module.

Although one embodiment of the invention has been described above, the programmable logic circuit control apparatus according to the invention can be realized by using an ordinary computer system, not an exclusive system. For example, as programs for

executing the operations of the module memory section 2, the module address memory section 3 and the circuit control section 4 are loaded from a medium (CD-ROM, MO or the like) where the programs are stored and installed in a computer connected to the programmable logic circuit 1, the computer functions as the programmable logic circuit control apparatus that executes the above-described processes.

A method of providing a computer with the programs is not limited. For example, programs may be uploaded to a BBS (Bulletin Board System) of a communication circuit, and distributed to the computer via the communication circuit. Alternatively, each program may be transmitted in a modulated wave which is a carrier wave modulated by a signal representing the program, and a unit which receives the modulated wave demodulates the modulated wave to restore the program. Then, the computer activates the program and executes the program in the same way as executing other application programs under the control of an OS (Operating System). This allows the computer to function as the programmable logic circuit control apparatus that executes the above-described processes.

When the OS is in charge of a part of a process, or the OS constitutes a part of a single structural element of the invention, a recording medium may store a program excluding that part. In this case, a program for executing individual functions or steps that a computer performs should be stored in the recording medium according to the invention.

Various embodiments and changes may be made thereunto without departing from the broad spirit and scope of the invention. The above-described embodiment is intended to illustrate the present invention, not to limit the scope of the present invention. The scope of the present invention is shown by the attached claims rather than the embodiment. Various modifications made within the meaning of an equivalent of the claims of the invention and within the claims are to be regarded to be in the scope of the present invention.

This application is based on Japanese Patent Application No. 2003-433210 filed on December 26, 2003 and including specification, claims, drawings and summary. The

disclosure of the above Japanese Patent Application is incorporated herein by reference in its entirety.

CLAIMS

1. A programmable logic circuit control apparatus comprising:

a controller (4) which supplies a control signal to an external programmable logic circuit (1) having a function of changing a logic configuration in accordance with a supplied control signal;

a module storage memory (2) which stores a plurality of modules each comprised of data defining a logic configuration of said programmable logic circuit (1); and

a module usage order designation memory (3) which has a plurality of ordered memory positions, each of the memory positions storing data for designating an address of a memory position of said module storage memory (2) in which a module to be executed is stored or storing data for designating an address of another memory position of this module usage order designation memory (3),

wherein said controller (4) acquires data stored at a memory position in said module usage order designation memory (3),

determines which of an address of the memory position storing the module and an address of the another memory position is designated by acquired data,

when having determined that said acquired data designates an address of the module, acquires said module stored in a memory position indicated by said address from said module storage memory (2), generates a control signal which controls said programmable logic circuit (1) to take a logic configuration defined by said module and supplies generated control signal to said programmable logic circuit (1), and

when having determined that said acquired data designates another memory position, acquires data stored at said another memory position from said module usage order designation memory (3).

2. The programmable logic circuit control apparatus according to claim 1, wherein when data stored at a memory position in said module usage order designation memory (3)

designates another memory position in said module usage order designation memory (3), said data includes condition definition data designating a condition to start a process of acquiring data stored at said another memory position, and

said controller (4) determines whether a condition designated by said condition definition data included in said acquired data is fulfilled or not when having determined that said acquired data designates another memory position,

acquires data stored at said another memory position of said module usage order designation memory (3) when having determined said condition is fulfilled, and

aborts acquisition of data at said another memory position when having determined that said condition is not fulfilled.

3. The programmable logic circuit control apparatus according to claim 2, wherein said condition designated by said condition definition data relates to a value given by a signal which is generated at a predetermined node of said programmable logic circuit (1), and

when having determined that data stored at a memory position in said module usage order designation memory (3) designates another memory position, said controller (4) acquires said signal from said node of said programmable logic circuit (1), and determines based on said value given by said acquired signal whether that condition which is designated by said condition definition data included in said data acquired from said module usage order designation memory (3) is fulfilled or not.

4. The programmable logic circuit control apparatus according to claim 1, wherein data stored at a memory position in said module usage order designation memory (3) includes identification data for identifying which one of an address of the memory position storing a module and an address of another memory position is designated by said stored data,

said controller (4) determines based on said identification data included in said data

acquired from said module usage order designation memory (3) which of an address of the memory position storing the module and an address of the another memory position is designated.

5. A programmable logic circuit control apparatus that acquires a module comprised of data defining a logic configuration of an external programmable logic circuit (1) having a function of changing a logic configuration in accordance with a supplied control signal from a module storage memory (2) which stores a plurality of modules, generates a control signal which controls said programmable logic circuit (1) to take a logic configuration defined by said acquired module and supplies generated control signal to said programmable logic circuit (1), and that comprises:

means which acquires data stored at a memory position in an external module usage order designation memory (3) which has a plurality of ordered memory positions, each of the memory position storing data for designating an address of a memory position of said module storage memory (2) in which a module to be executed is stored or storing data for designating an address of another memory position of this module usage order designation memory (3), from said module usage order designation memory (3);

means which determines which of an address of the memory position storing the module and an address of the another memory position is designated by acquired data;

means which, when it is determined that said acquired data designates an address of the module, acquires said module stored in a memory position indicated by said address from said module storage memory (2), and changes said logic configuration of said programmable logic circuit (1) so that said programmable logic circuit (1) takes a logic configuration defined by said module; and

means which, when it is determined that said acquired data designates another memory position, acquires data stored at said another memory position from said module usage order designation memory (3).

6. A programmable logic circuit control method which supplies a control signal to an external programmable logic circuit (1) having a function of changing a logic configuration in accordance with said supplied control signal, and comprises the steps of:

storing a plurality of modules each comprised of data defining a logic configuration of said programmable logic circuit (1);

storing data for designating an address of a memory position storing a module or an address of another memory position at each of a plurality of ordered memory positions;

acquiring data stored at each of said memory positions;

determining which of an address of the memory position storing the module and an address of the another memory position is designated by the acquired data;

when it is determined that said acquired data designates an address of a memory position storing a module, acquiring said module stored in the memory position indicated by said address, generating a control signal which controls said programmable logic circuit (1) to take a logic configuration defined by said module and supplying said control signal to said programmable logic circuit (1); and

when it is determined that said acquired data designates an address of another memory position, acquiring data stored at said another memory position.

7. A programmable logic circuit control method that acquires a module comprised of data defining a logic configuration of an external programmable logic circuit (1) having a function of changing a logic configuration in accordance with a supplied control signal from a module storage memory (2) which stores a plurality of modules, generates a control signal which controls said programmable logic circuit (1) to take a logic configuration defined by said acquired module and supplies said control signal to said programmable logic circuit (1), and that comprises the steps of:

acquiring data stored at a memory position in an external module usage order designation memory (3) which has a plurality of ordered memory positions, each of the

memory positions storing data for designating an address of a memory position of said module storage memory (2) in which a module to be executed is stored or storing data for designating an address of another memory position of this module usage order designation memory (3);

determining which of an address of the memory position storing the module and an address of the another memory position is designated by the acquired data;

when it is determined that said acquired data designates an address of a memory position storing a module, acquiring said module stored in the memory position indicated by said address from said module storage memory (2), and changing said logic configuration of said programmable logic circuit (1) so that said programmable logic circuit (1) takes a logic configuration defined by said module; and

when it is determined that said acquired data designates another memory position, acquiring data stored at said another memory position from said module usage order designation memory (3).

8. A program for allowing a computer to function as:

a controller (4) which supplies a control signal to an external programmable logic circuit (1) having a function of changing a logic configuration in accordance with said supplied control signal;

a module storage memory (2) which stores a plurality of modules each comprised of data defining a logic configuration of said programmable logic circuit (1); and

a module usage order designation memory (3) which has a plurality of ordered memory positions, each of the memory positions storing data for designating an address of a memory position of said module storage memory (2) in which a module to be executed is stored or storing data for designating an address of another memory position of the module usage order designation memory (3),

wherein said controller (4) acquires data stored at a memory position in said module

usage order designation memory (3),

determines which of an address of the memory position storing the module and an address of the another memory position is designated by the acquired data,

when having determined that said acquired data designates an address of a module, acquires said module stored in a memory position indicated by said address from said module storage memory (2), generates a control signal which controls said programmable logic circuit (1) to take a logic configuration defined by said module and supplies the generated control signal to said programmable logic circuit (1), and

when having determined that said acquired data designates another memory position, acquires data stored at said another memory position from said module usage order designation memory (3).

9. A program for allowing a computer to function as a programmable logic circuit control apparatus that acquires a module comprised of data defining a logic configuration of an external programmable logic circuit (1) having a function of changing a logic configuration in accordance with a supplied control signal from a module storage memory (2) which stores a plurality of modules, generates a control signal which controls said programmable logic circuit (1) to take a logic configuration defined by said acquired module and supplies generated control signal to said programmable logic circuit (1), and for further allowing said computer to perform the functions of:

acquiring data stored at a memory position in an external module usage order designation memory (3) which has a plurality of ordered memory positions, each of the memory positions storing data for designating an address of a memory position of said module storage memory (2) in which a module to be executed is stored or storing data for another memory position of this module usage order designation memory (3);

determining which of an address of the memory position storing the module and an address of the another memory position is designated by acquired data;

when it is determined that said acquired data designates an address of a module, acquiring said module stored in a memory position indicated by said address from said module storage memory (2), and changing said logic configuration of said programmable logic circuit (1) so that said programmable logic circuit (1) takes a logic configuration defined by said module; and

when it is determined that said acquired data designates another memory position, acquiring data stored at said another memory position from said module usage order designation memory (3).

FIG.1

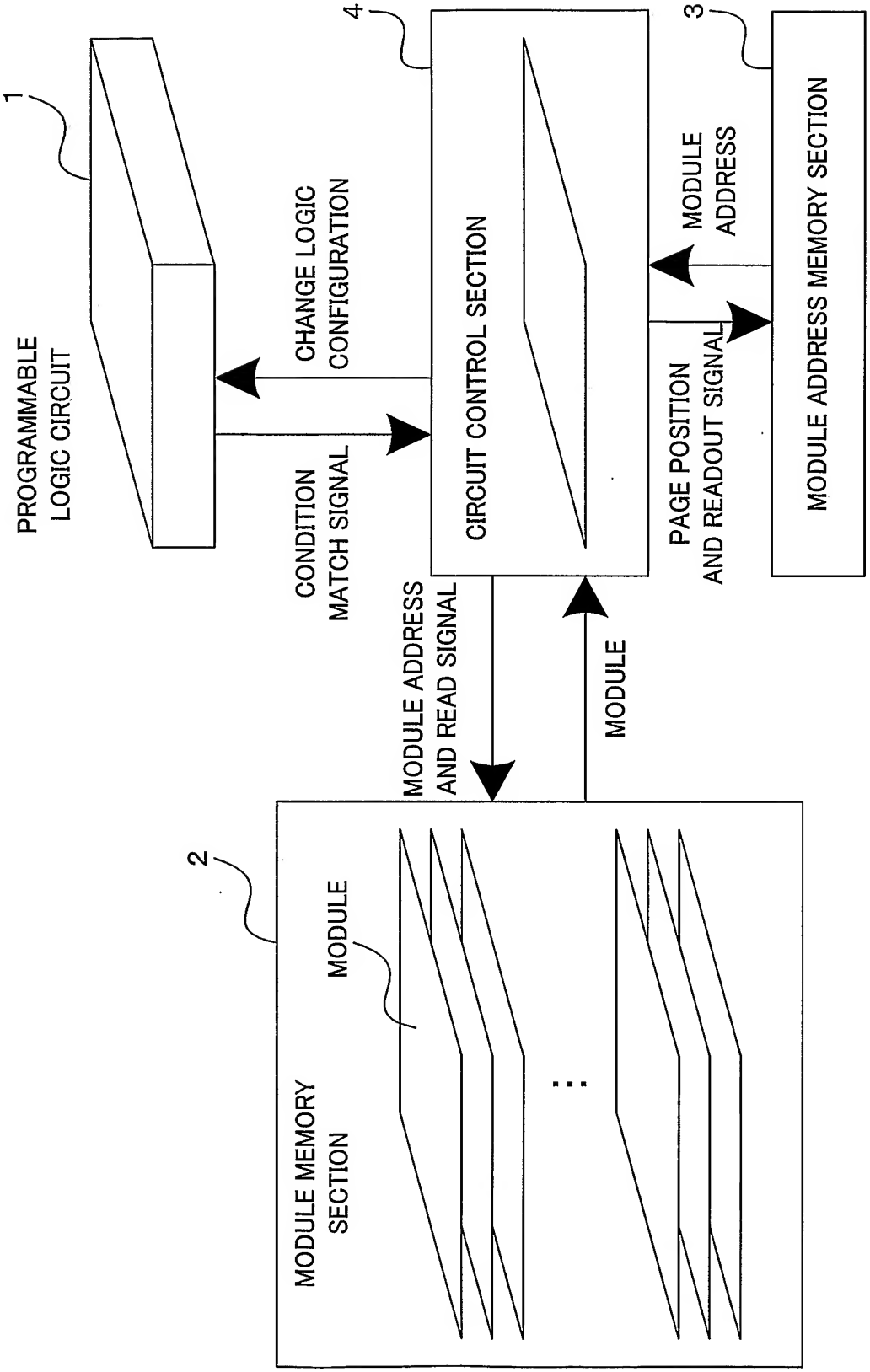

1
PROGRAMMABLE LOGIC CIRCUIT
CHANGE LOGIC CONFIGURATION
CONDITION MATCH SIGNAL
4
CIRCUIT CONTROL SECTION
MODULE ADDRESS
PAGE POSITION AND READOUT SIGNAL
3
MODULE ADDRESS MEMORY SECTION
MODULE ADDRESS AND READ SIGNAL
MODULE
2
MODULE MEMORY SECTION
MODULE

FIG.2

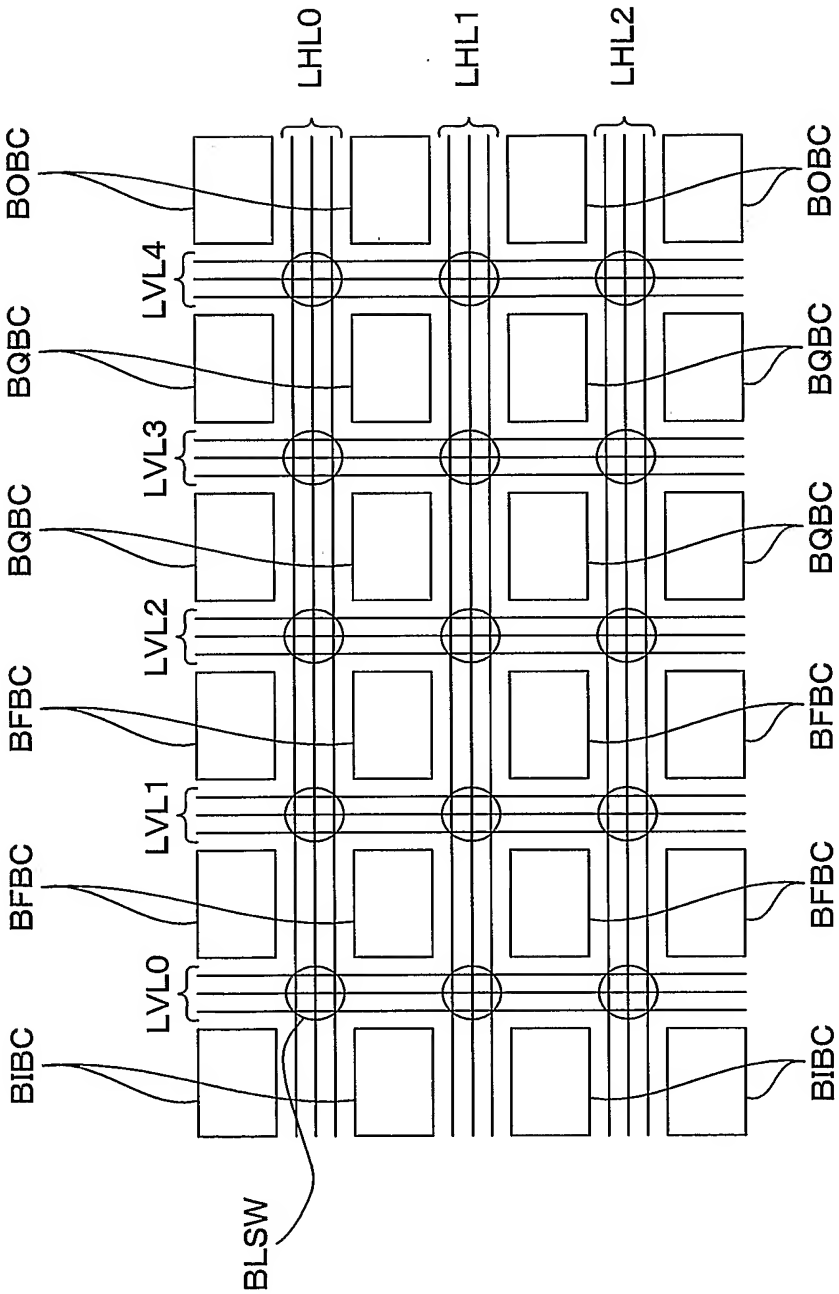

LHL0
LHL1
LHL2
BOBC
BQBC
BQBC
BFBC
BFBC
BIBC
LVL4
LVL3
LVL2
LVL1
LVL0
BLSW

FIG.3

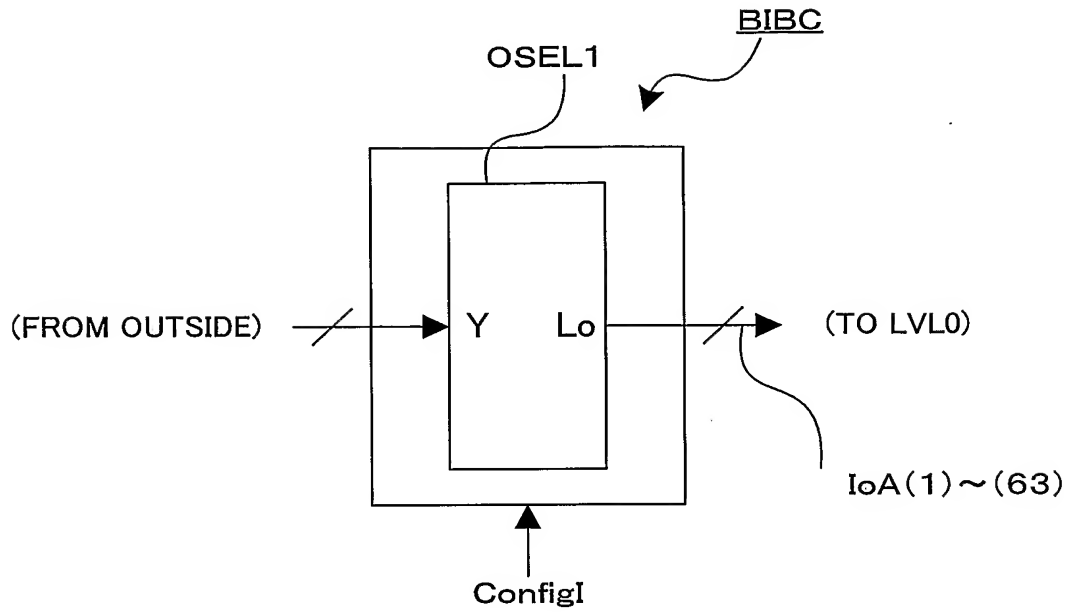

BIBC
OSEL1
(FROM OUTSIDE)
Y
Lo
(TO LVL0)
IoA(1)～(63)
ConfigI

FIG.4

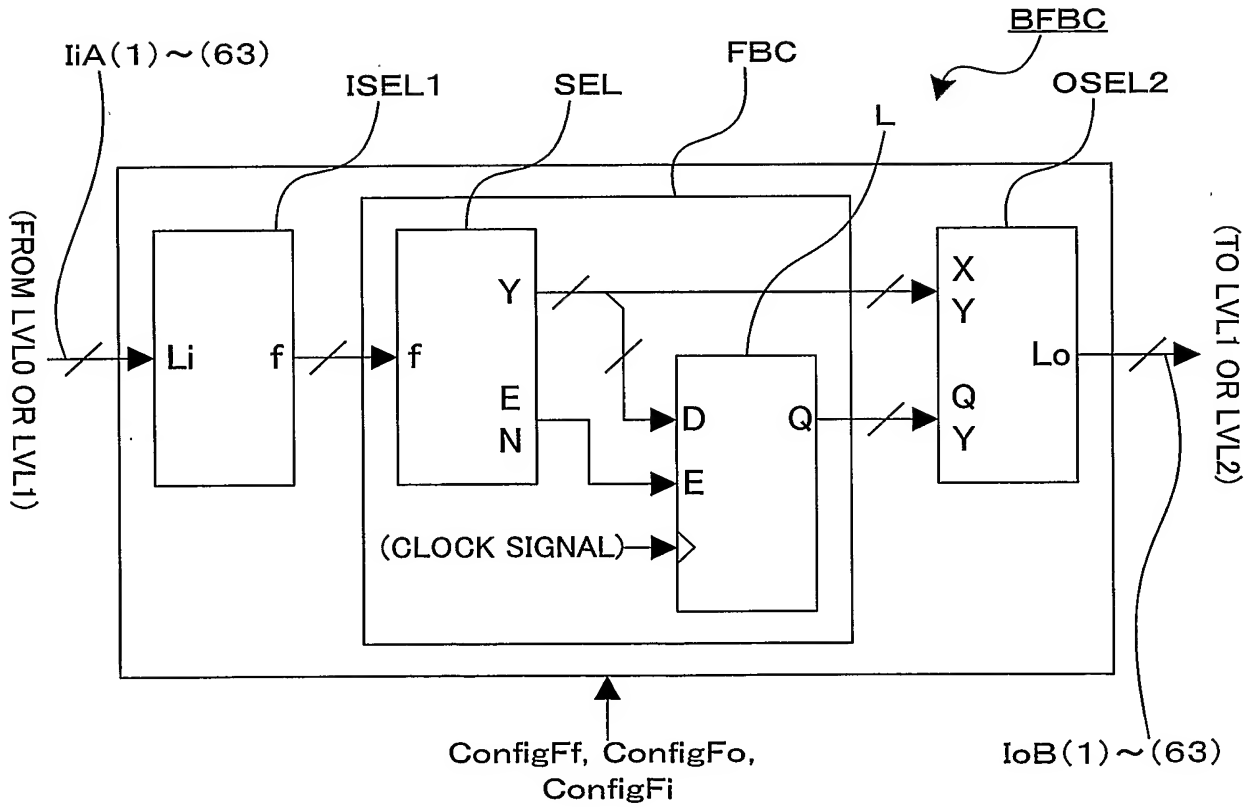

BFBC
IiA(1)～(63)
ISEL1
SEL
FBC
L
OSEL2
(FROM LVL0 OR LVL1)
Li
f
f
Y
E
N
D
Q
E
(CLOCK SIGNAL)
X
Y
Q
Y
Lo
(TO LVL1 OR LVL2)
ConfigFf, ConfigFo,
ConfigFi
IoB(1)～(63)

FIG.5

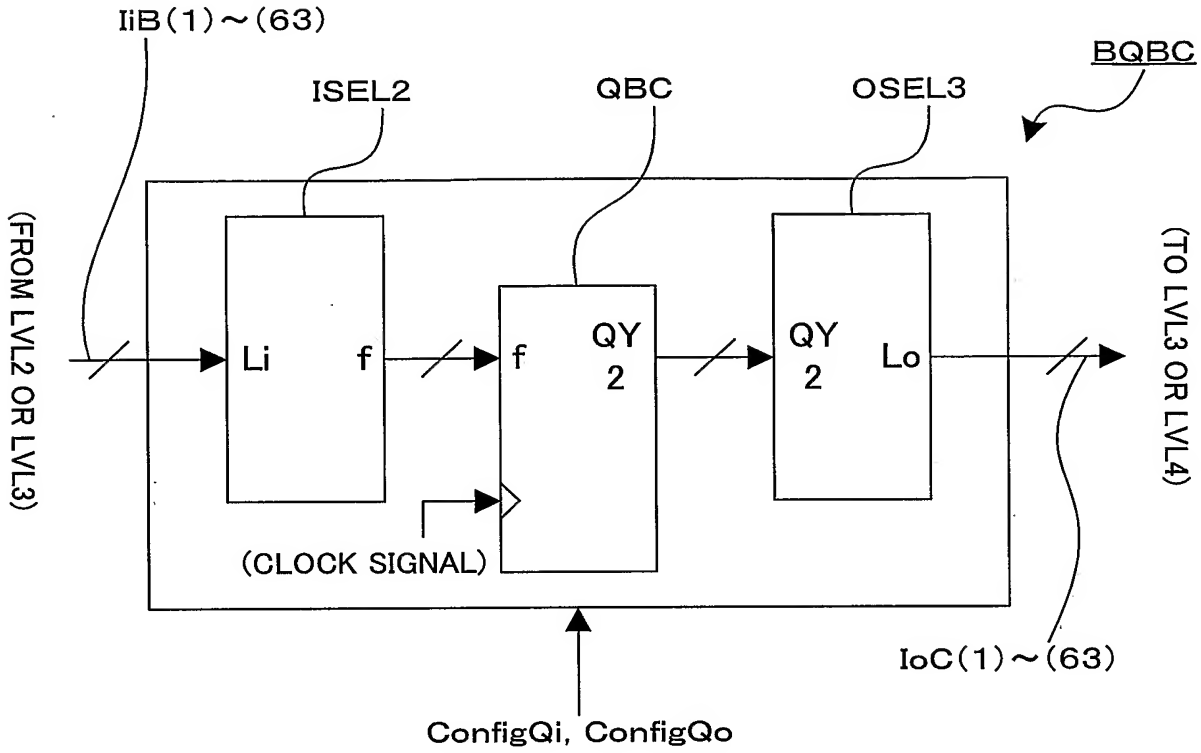

IiB(1)～(63)
BQBC
ISEL2
QBC
OSEL3
(FROM LVL2 OR LVL3)
Li
f
f
QY
2
QY
2
Lo
(TO LVL3 OR LVL4)
(CLOCK SIGNAL)
IoC(1)～(63)
ConfigQi, ConfigQo

FIG.6

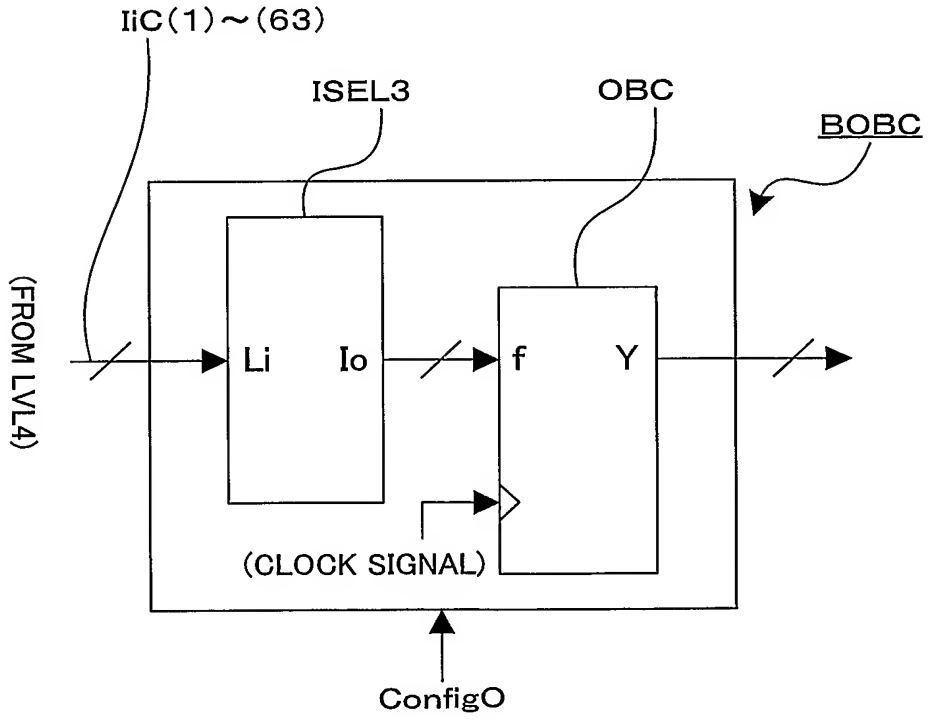

IiC(1)～(63)
ISEL3
OBC
BOBC
(FROM LVL4)
Li
Io
f
Y
(CLOCK SIGNAL)
ConfigO

FIG.7A

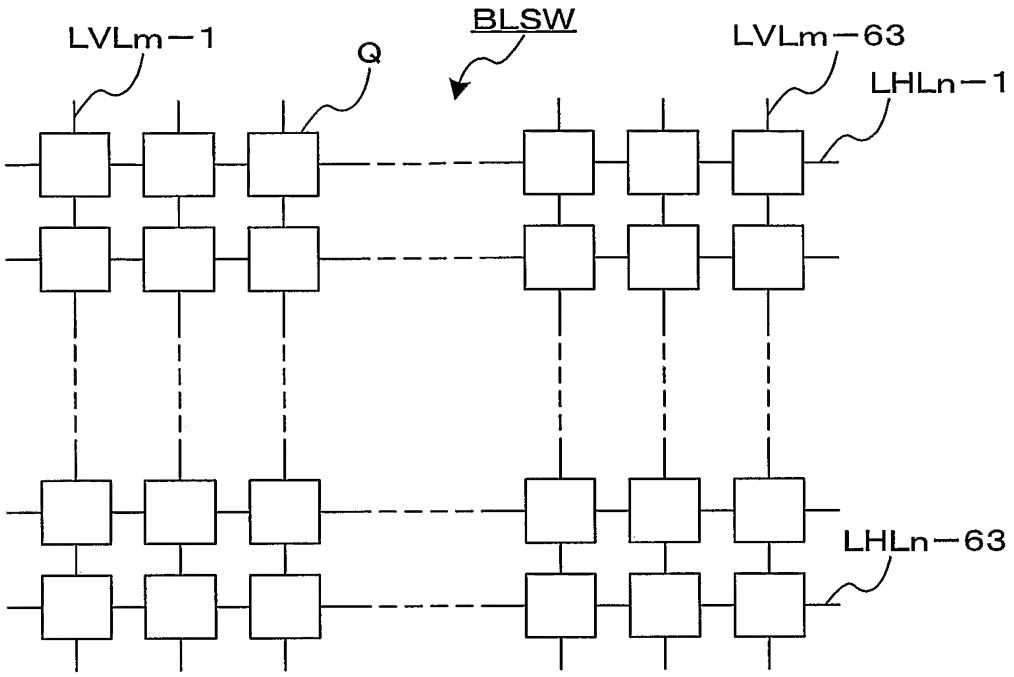

LVLm−1
Q
BLSW
LVLm−63
LHLn−1
LHLn−63

FIG.7B

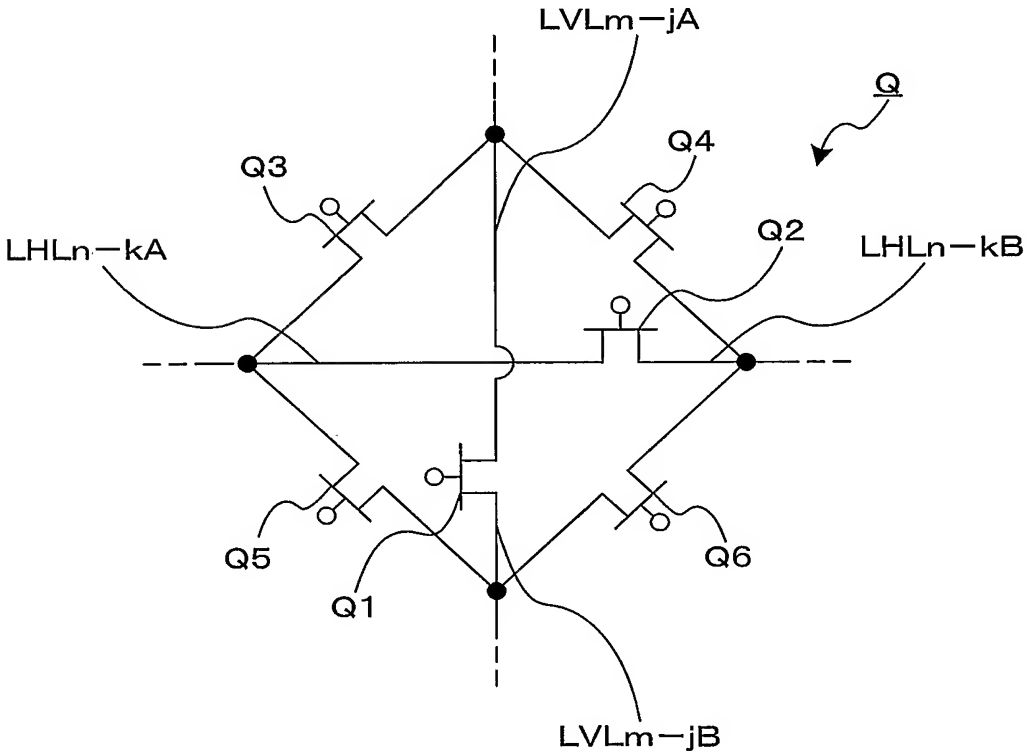

LVLm−jA
Q
Q4
Q3
Q2
LHLn−kA
LHLn−kB
Q5
Q6
Q1
LVLm−jB

FIG.8

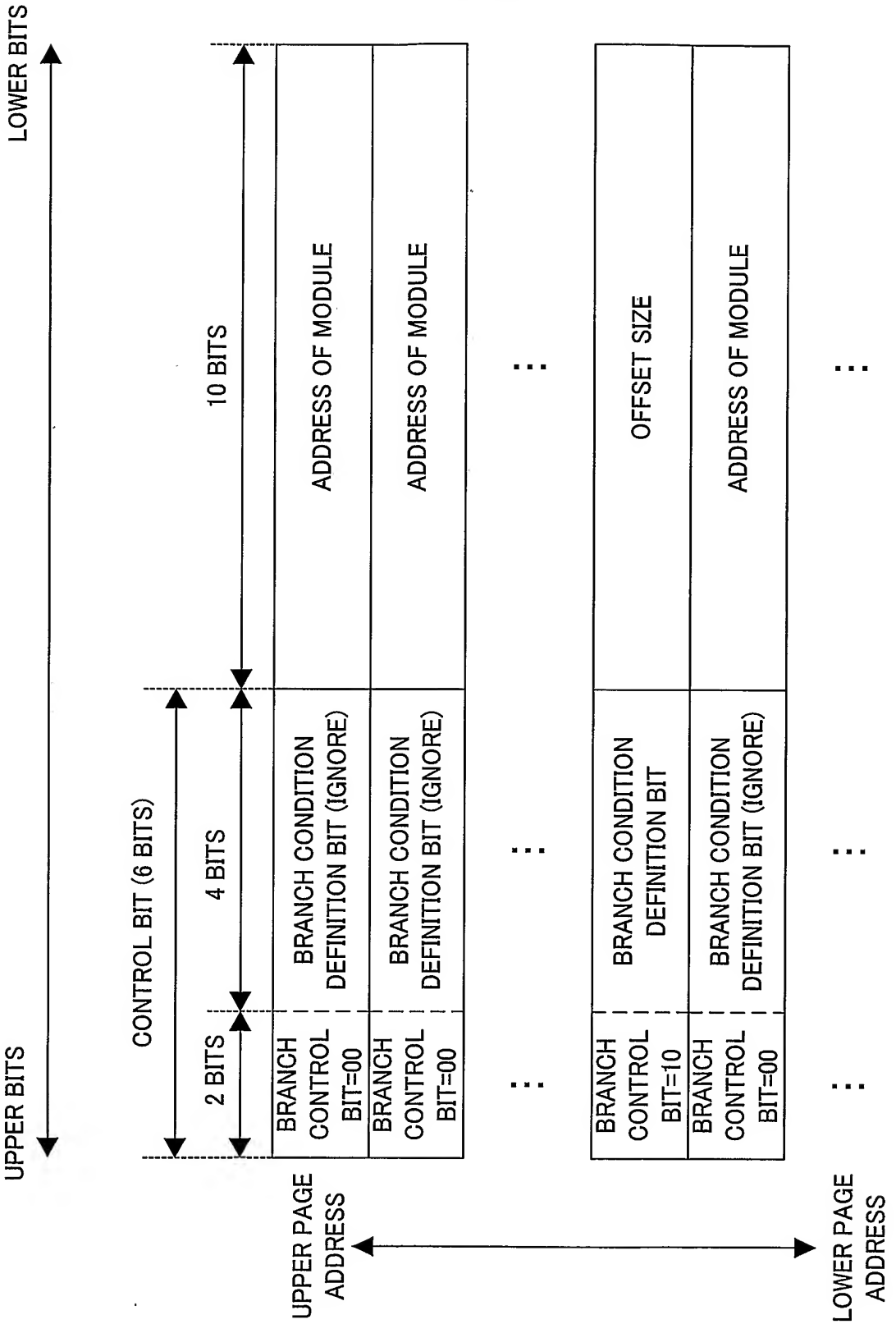
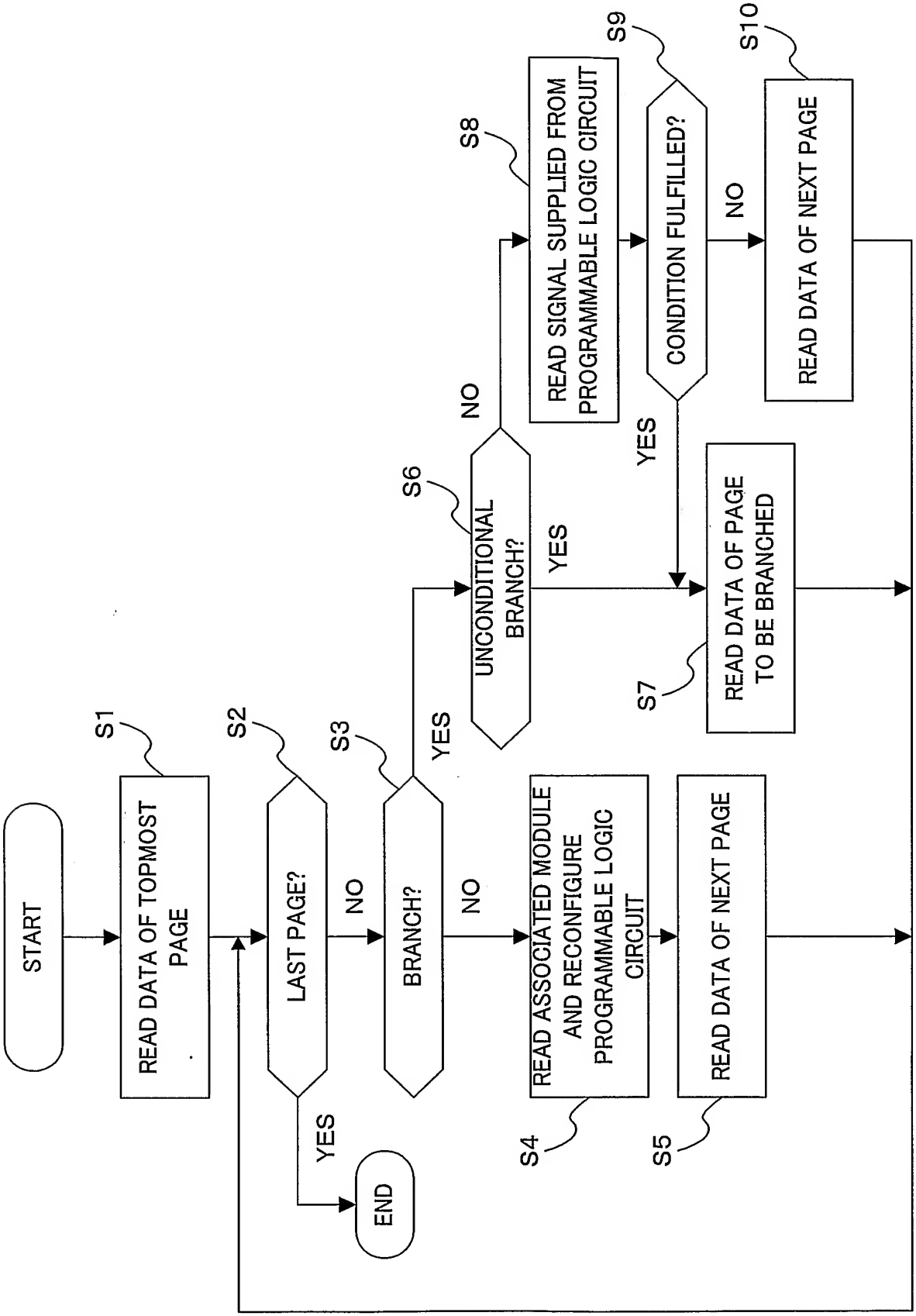

LOWER BITS
UPPER BITS
CONTROL BIT (6 BITS)
2 BITS
4 BITS
10 BITS
BRANCH CONTROL BIT=00
BRANCH CONDITION DEFINITION BIT (IGNORE)
ADDRESS OF MODULE
BRANCH CONTROL BIT=00
BRANCH CONDITION DEFINITION BIT (IGNORE)
ADDRESS OF MODULE
BRANCH CONTROL BIT=10
BRANCH CONDITION DEFINITION BIT
OFFSET SIZE
BRANCH CONTROL BIT=00
BRANCH CONDITION DEFINITION BIT (IGNORE)
ADDRESS OF MODULE
UPPER PAGE ADDRESS
LOWER PAGE ADDRESS

FIG.9


START
READ DATA OF TOPMOST PAGE
S1
LAST PAGE?
S2
YES
END
NO
BRANCH?
S3
YES
NO
UNCONDITIONAL BRANCH?
S6
YES
NO
READ ASSOCIATED MODULE AND RECONFIGURE PROGRAMMABLE LOGIC CIRCUIT
S4
READ DATA OF NEXT PAGE
S5
READ DATA OF PAGE TO BE BRANCHED
S7
READ SIGNAL SUPPLIED FROM PROGRAMMABLE LOGIC CIRCUIT
S8
CONDITION FULFILLED?
S9
YES
NO
READ DATA OF NEXT PAGE
S10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2004/019819

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl[7] G06F 9/30, H03K 19/173

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl[7] G06F 9/30, H03K 19/173

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Japanese Utility Model Gazette 1922-1996, Japanese Publication of Unexamined Utility Model Applications 1971-2005, Japanese Registered Utility Model Gazette 1994-2005, Japanese Gazette Containing the Utility Model 1996-2005

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 11-296345 A (HITACHI LTD.) 1999.10.29, [0076],Fig.8 (no family)	1 - 9
A	JP 2001-68993 A(FUJI XEROX CO. LTD.) 2001.03.16,[0042]-[0043],Fig.4(no family)	1 - 9

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16.03.2005	05.4.2005

Name and mailing address of the ISA/JP	Authorized officer
Japan Patent Office 3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	AKIRA GOTO Telephone No. +81-3-3581-1101 Ext. 3545

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